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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,163	02/11/2004	Stephan P. Kudelka	INF-106	1213
27896	7590	03/25/2005	EXAMINER	
EDELL, SHAPIRO, FINNAN & LYTLE, LLC 1901 RESEARCH BOULEVARD SUITE 400 ROCKVILLE, MD 20850				RAO, SHRINIVAS H
		ART UNIT		PAPER NUMBER
		2814		

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/775,163	KUDELKA, STEPHAN P.
Examiner	Art Unit	
Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 March 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) 1-9 and 16-18 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 10-15 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 11 February 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
Paper No(s)/Mail Date: _____	6) <input type="checkbox"/> Other: _____

Priority

The application as currently filed does not claim priority from any previously filed Application. Therefore currently the earliest available filing date is the U.S. filing date namely February 11, 2004.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-9 and 16-18 , are drawn to a method of forming a storage capacitor , classified in class 438 , subclass 260 +.
- II. Claim s 10-15, are drawn to DRAM array , classified in class 257 , subclass 317 +.

The inventions are distinct, each from the other because:

Inventions Gr. I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)).

In the instant case the process as claimed can be used to make other and materially different product namely a deep trench structure that need not be a capacitor having a bottle shaped cross section.

Because these inventions are distinct for the reasons given above and the search required for Group i is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Patrick Finn, Esq. (R.No. 39,189) on Friday March 11, 2005 and March 16, 2005 a provisional election was made with out traverse to prosecute the invention of Gr. II, claims 10-15.

Affirmation of this election must be made by applicant in replying to this Office action.

Claims 1-9 and 16-18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

It is requested that Applicants' cancel nonelected claims 1-9 and 16-18 at the earliest opportunity.

Information Disclosure Statement

No IDS to date has been filed.

Drawings

Figures 1a, 1b, 2,3 and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11 and its depended claims 12-15 and verb “steps of forming” directed to neither a “process” nor a “machine,” but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. *Ex parte Lyell*, 17 USPQ2d 1548, 1551 (Bd. Pat. App. & Inter. 1990). Claim 10 recites An array of DRAM capacitors while dependent claims 11-15 all recite steps of forming the array .

A claim which claims both an apparatus and method steps of using the apparatus is indefinite. *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiao et al. (U.S. Patent No. 6,365,485, herein after Shiao) in view of Chen (U.S. Patent No. 5, 702,968, herein after Chen).

With respect to claim 10 Shiao describes an array of DRAM trench capacitors, (Shiao col. 3 line 1, etc.) wherein each trench capacitor has a bottle shaped trench cross-section of substantially uniform shape when viewed in cross-section, (figures 2a –g , col. 3 lines 10-11, col. 8 lines 10-60).

Shiao does not specifically describe wherein the uniformity of bottle trench dimensions does not vary substantially among capacitors within the array.

However , Chen a patent from the same filed of endeavor describes in col. 3 lines 45 to 54 describes the uniformity of bottle trench dimensions does not vary substantially among capacitors within the array to provide a method for forming capacitors with high reliability and large cell capacitance and the device so formed. . (Chen col. 3 lines 45-55).

Therefor it would have been obvious to one of ordinary skill in the art at the time of the invention to include Chen's the uniformity of bottle trench dimensions does not vary substantially among capacitors within the array in Shiao's device/method. The motivation to make the above combination is to provide a method for forming capacitors with high reliability and large cell capacitance and the device so formed. . (Chen col. 3 lines 45-55).

With respect to claim 11, to the extent understood, Shiao describes the array of claim 10, wherein the steps for forming the array include : forming an

initial deep trench structure in a silicon substrate through an etching process, (Shiao col. 6 lines7-10,) forming a sacrificial doped silicon layer extending from a surface of an interior of said deep trench into the silicon substrate,(Shio col. 6 lines 36-40) resulting in an internal p-type silicon/silicon interface; (Shiao col. 6 line40 arsenic-p-type dopant) selectively removing said sacrificial doped silicon layer from said trench interior surface; (Shao figures 2F- 2G bottom part of 206 b removed) forming a buried plate electrode, (Shiao fig. 2g # 216) capacitor dielectric, (Shiao fig. 2H #218a) and top electrode.(Shiao figure 2 H 3 220, col. 9 lines 15-24).

At the outset it is noted that claims 11 and its depended claims 12-15 and verb " steps of forming " directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. *Ex parte Lyell*, 17 USPQ2d 1548, 1551 (Bd. Pat. App. & Inter. 1990). Claim 10 recites An array of DRAM capacitors while dependent claims 11-15 all recite steps of forming the array . A claim which claims both an apparatus and method steps of using the apparatus is indefinite. *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990).(see above also) .

With respect to claim 12 to the extent understood, Shiao describes the array of claim 11, (Shiao col. 6 line40 arsenic-p-type dopant).

With respect to claim 13 to the extent understood, Shiao describes the array of claim 12, wherein said p-doped silicon layer is formed by gas phase doping. (Shiao col. 6 line36-37, etc.).

With respect to claim 14 to the extent understood, Shiao describes the array of claim 11, wherein said selectively removing said sacrificial doped silicon layer comprises : forming an n-type region extending from said internal p-type silicon interface further into said silicon substrate, (Shiao col. 9 lines10-15, # 222 not shown in figures) and selectively etching said p-type layer such that said n-type region remains substantially unetched during said selectively etching said p-type layer.(Shiao col. 9 lines 4-8, only first conductive layer 220 a is etched before forming second conductive material).

With respect to claim 15 to the extent understood, Shiao describes the array of claim 14, wherein said selectively etching said p-type layer is performed by chemical etching using an aqueous solution of hydroxide of potassium or ammonia, (Shiao col. 9 line 6 etching, KOH/Ammonia well known etchant for RIE, BOE and combined etching systems – e.g. Peter Van Sant , 4 edn. Pages 260, and 270,) further comprising the step of applying a bias voltage to said p-type layer during said chemical etching. 9 Eg. Peter Van Zant page 269). The motivation to refer to well known text books is to find what the state of the art is in similar process/devices.) .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1781. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Steven H. Rao
Patent Examiner

March 21, 2005.